

FIG. 1A

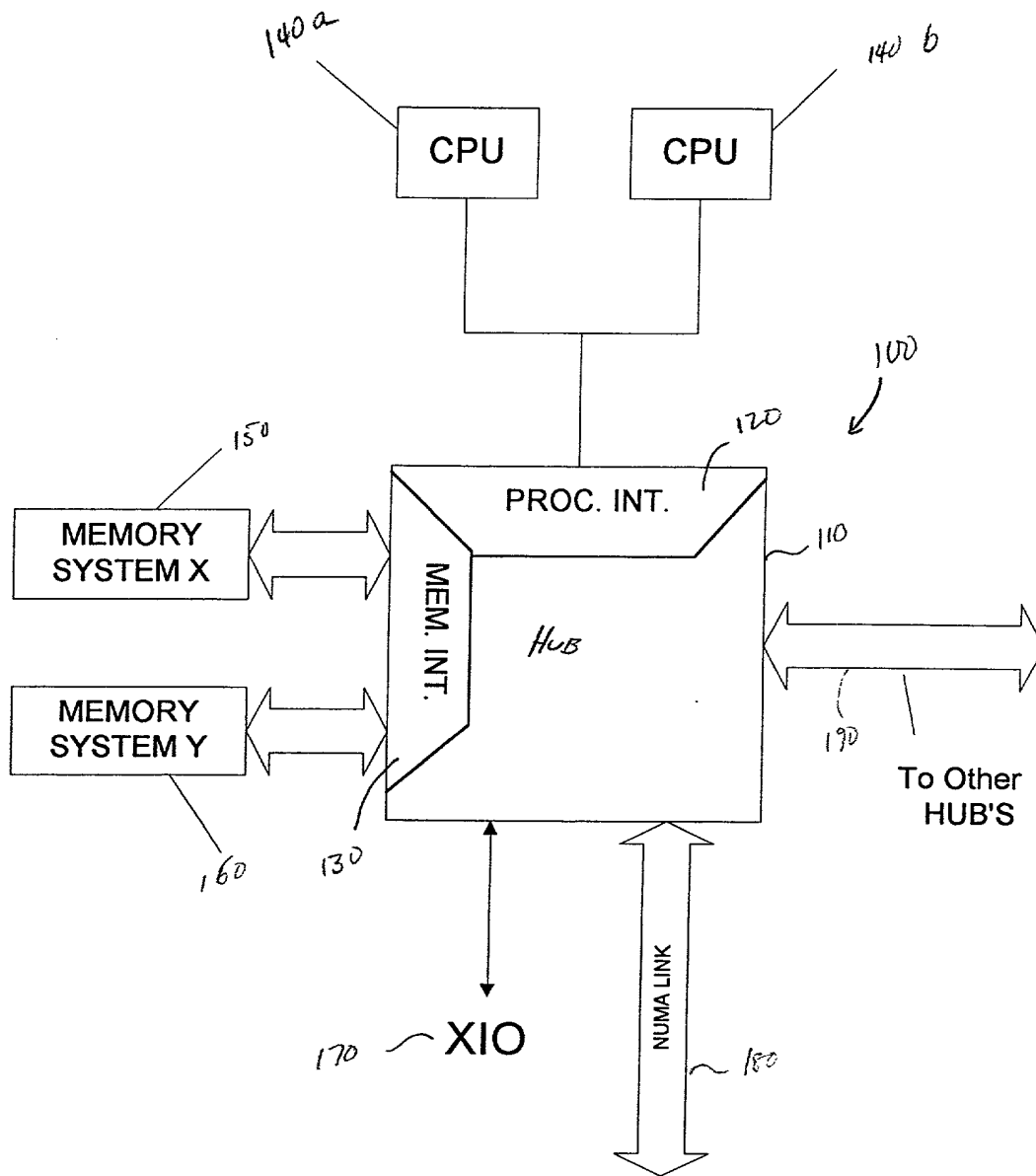
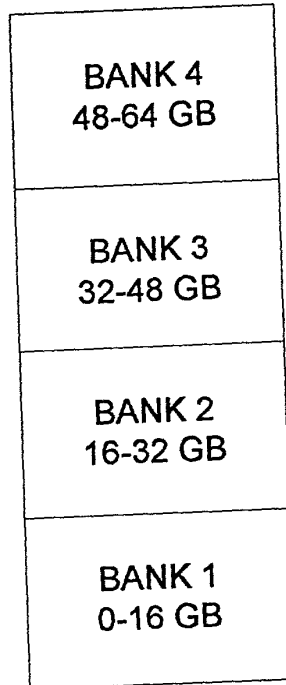


FIG. 1B



36 BIT MEMORY ADDRESS

BITS 35:34 - BANK SELECT
BITS 33:0 - ADDRESS WITHIN BANK

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FIG 2A

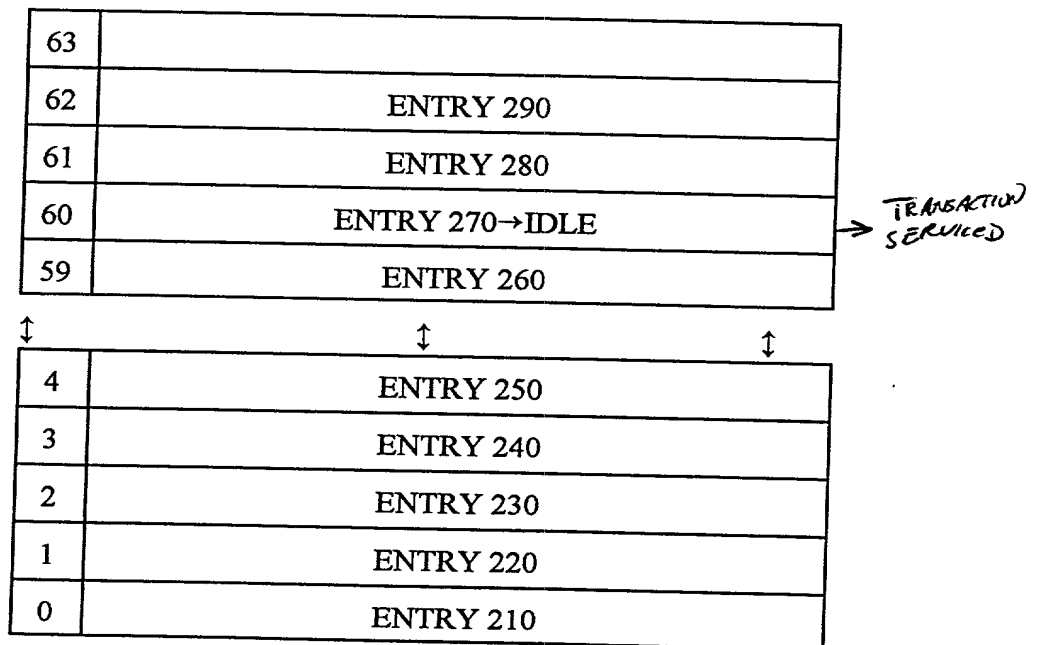
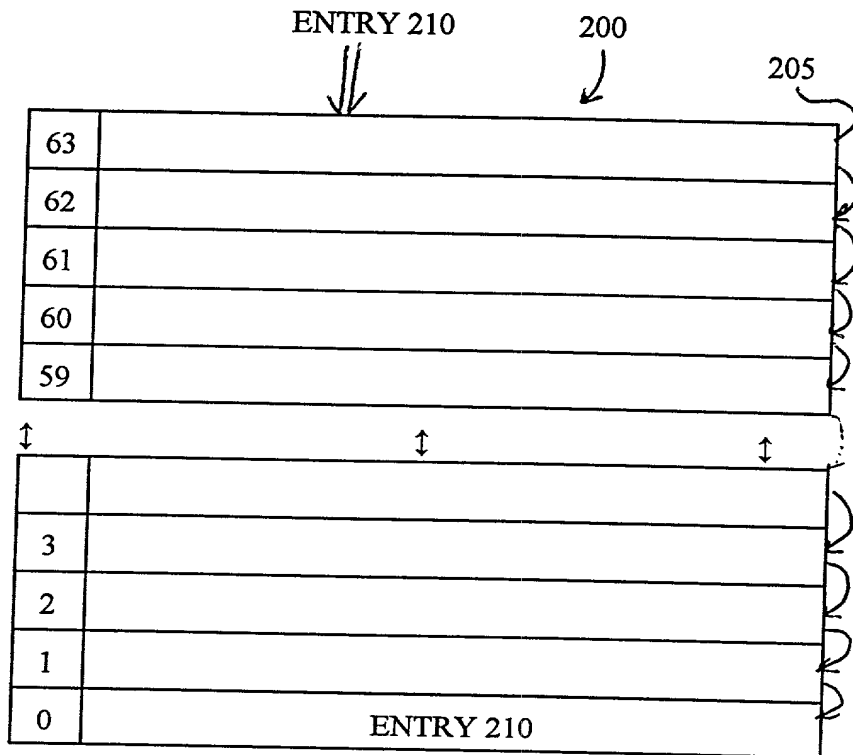


FIG. 2B

63	
62	
61	ENTRY 290
60	ENTRY 280
59	ENTRY 260

↑ ↑ ↑

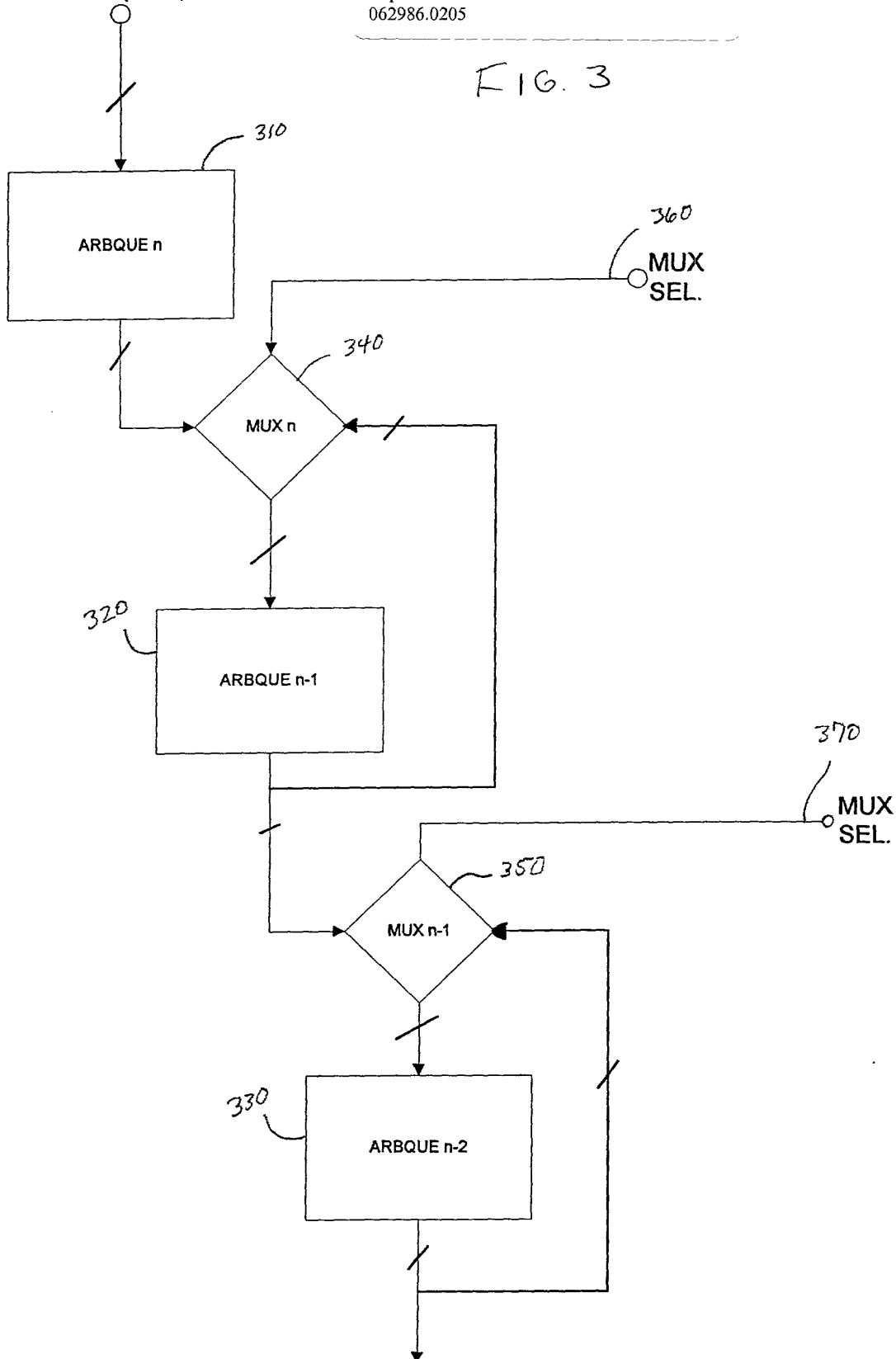
4	ENTRY 250
3	ENTRY 240
2	ENTRY 230
1	ENTRY 220
0	ENTRY 210

FIG 4.

STATE	R/W	CHAIN OK	BANK FREE	OP READY	TRANSACTION
460	450	440	430	420	410

FIG. 3

FROM MUX (n + 1)

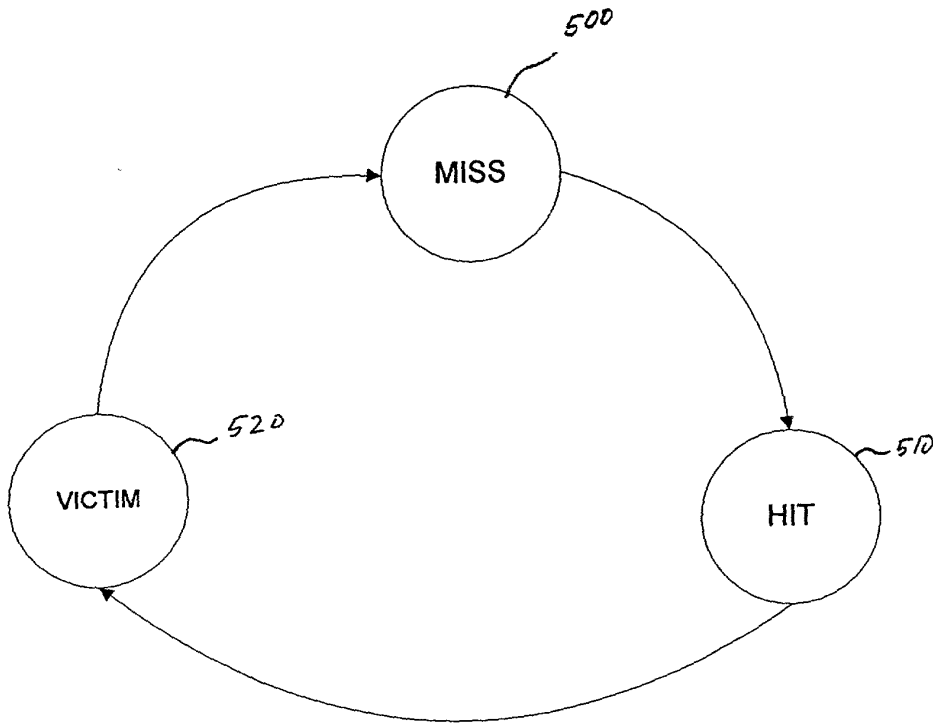


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QUEUE CIRCUIT AND METHOD FOR
MEMORY ARBITRATION EMPLOYING
SAME

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FIG 5



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FIG. 6

600 610 620 630 640 650 660

DRAM Direction Arbitration Policy Table

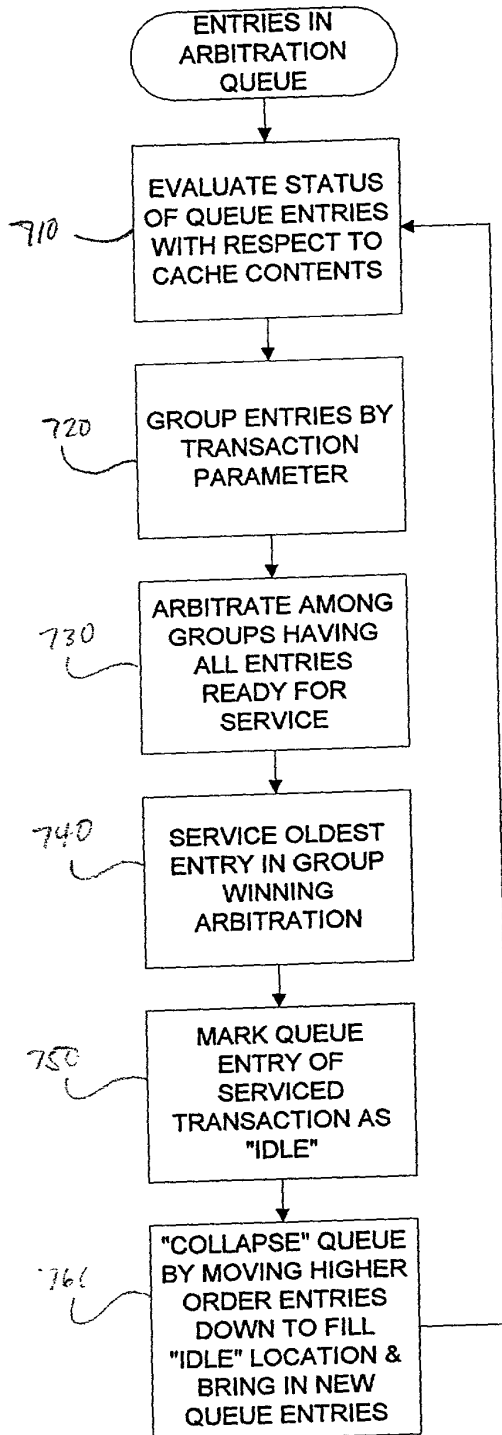
Read	Write	Urgent Write	Follows Read	Follows Write	Direction Threshold	Arbitrate For
x	0	0	x	x	x	Read
0	x	1	x	x	x	Write
0	1	0	1	0	x	Read
0	1	0	0	x	x	Write
1	1	0	x	0	x	Read
1	1	0	0	1	0	Write
1	1	0	0	1	1	Read
1	x	1	0	x	x	Write
1	x	1	1	0	0	Read
1	x	1	1	0	1	Write

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FIG 7



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